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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,674	11/24/2003	Ming-Hsuan Chang	MR3029-82	1648

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,674	CHANG, MING-HSUAN	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-11 and 13-15* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 01/27/2005 has been entered.

Drawings

2. The drawings were previously objected to as failing to comply with 37 CFR 1.83(a) and 37 CFR 1.84(p)(4). Due to changes made in the specification, and cancellation of claim 6, these objections no longer apply.

3. The formal drawings filed on 11/24/2003 are acceptable.

Information Disclosure Statement

4. If applicant is aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Busta (4,859,623).

Busta discloses a transistor comprising a first conducting structure 22C, for example, a signal/data line, upon a substrate 10; a second conducting structure 14A, for example a scanning/gate line, upon said substrate 10, with the projection of said second conducting structure (scanning/gate line 14A) onto said substrate 10 intersecting the projection of said first conducting structure (signal/data line 22C) onto said substrate 10; a third conducting structure 22B, for example a source electrode, upon said substrate 10 contacting with said first conducting structure (signal/data line 22C), with the projection of said third conducting structure (source electrode 22B) onto said substrate 10 separated from said projection of said second conducting structure (scanning/gate line 14A) onto said substrate 10; a fourth conducting structure 14, for example a gate, upon said substrate 10 contacting with said second conducting structure (scanning/gate line 14A), with the projection of said fourth conducting structure (gate 14) onto said substrate 10 separated from said projection of said first conducting structure (signal/data line 22C) onto said substrate 10, and said fourth conducting structure (gate 14) intersecting (figure reference elements 24 show the intersection between gate 14 and the projection of source electrode 22B, as well as the overlap between the projections of gate 14 and drain electrode 22A. Note column 3 lines 47-50 of the text) the projection of said third conducting structure (source electrode 22B) onto said substrate 10; a fifth conducting structure 22A, for example a drain electrode, upon said substrate 10, with the projection

of said fifth conducting structure (drain electrode 22A) onto said substrate 10 at least partly overlapping said projection (figure reference elements 24 show the overlap between the projections of gate 14 and drain electrode 22A, as well as the intersection between the projections of gate 14 and source electrode 22B. Note column 3 lines 47-50 of the text) of said fourth conducting structure (gate 14) onto said substrate 10 and separated from said projection of said third (source electrode 22B), said first (signal/data line 22C), and said second conducting structure (scanning/gate line 14A) onto said substrate 10; and a semiconductor layer 18A, for example a channel region, upon said substrate 10 and electrically coupling with said third (source electrode 22B) and said fifth (drain electrode 22A) conducting structures with the projection of said semiconductor layer (channel region 18A) onto said substrate 10 completely inside said projection of said fourth conducting structure (gate 14) onto said substrate 10, wherein said projections of said fifth (drain electrode 22A) and said second (scanning/gate line 14A) conducting structures onto said substrate 10 are on the opposite sides of said projection of said third conducting structure (source electrode 22B) onto said substrate 10, said projection of said fifth conducting structure (drain electrode 22A) onto said substrate 10 does not contact with the end of said projection of said fourth conducting structure (gate 14) onto said substrate 10 not contacting with said second conducting structure (scanning/gate line 14A, wherein said projection of said fifth conducting structure (drain electrode 22A) onto said substrate 10 is completely inside said projection of said fourth conducting structure (gate 14) onto said substrate 10, said projection of said fifth conduct-

ing structure (drain electrode 22A) onto said substrate 10 not completely inside said projection (some of the drain electrode 22A projection being inside, as indicated by reference 24, and the rest being outside the gate 14 projection) of said fourth conducting structure (gate 14) onto said substrate 10, said projection of said fifth conducting structure (drain electrode 22A) onto said substrate 10 not contacting with the end of said projection of said fourth conducting structure (gate 14) onto said substrate 10 not contacting with said second conducting structure (scanning/gate line 14A), the opposite two sides of said projection of said fifth conducting structure (drain electrode 22A) onto said substrate 10 passed by said projection of said fourth conducting structure (gate 14) onto said substrate 10 approximately parallel to one another at and near the intersecting area of said projection of said fourth (gate) and said fifth conducting structure (drain electrode 22A), and said projections of said fifth (drain, drain electrode, or pixel electrode) and said fourth (gate 14) conducting structures onto said substrate 10 being approximately parallelograms. Note figure 1 and column 3 lines 19-54 of Busta.

Claims 10,11, and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Morozumi (4,600,274).

With regard to claims 10 and 11 Morozumi discloses a transistor with a first conducting structure 43, for example, a signal/data line, upon a substrate 40; a second conducting structure 44, for example a scanning/gate line, upon said substrate 40, with the projection of said second conducting structure (scanning/gate line 44) onto said substrate 40 intersecting the projection of said first conducting structure (signal/data line 43) onto

said substrate 40; a third conducting structure 53, for example a source, upon said substrate 40 contacting with said first conducting structure (signal/data line 43), with the projection of said third conducting structure (source 53) onto said substrate 40 completely inside said projection of said second conducting structure (scanning/gate line 44) onto said substrate 40; and a fourth conducting structure 50, for example a gate, upon said substrate 40, with the projection of said fourth conducting structure (gate 50) onto said substrate 40 separated from said projection of said first (signal/data line 43) and said third conducting structure (source 53) onto said substrate 40, said projection of said fourth conducting structure (gate 50) onto said substrate 40 completely inside said projection of said second conducting structure (scanning/gate line 44) onto said substrate 40; and said projection of said fourth conducting structure (gate 50) onto said substrate 40 approximately parallel to said projection of said third conducting structure (source 53) onto said substrate 40; wherein the side of said projection of said fourth conducting structure (gate 50) onto said substrate 40 approximately parallel to said projection of said third conducting structure (source 53) onto said substrate 40 far longer than the side of said projection of said fourth conducting structure (gate 50) onto said substrate 40 approximately parallel to said projection of said first conducting structure (signal/data line 43) onto said substrate 40. Note figures 4a, 4c, and column 4 lines 15-36 and 54-68 of Morozumi.

With regard to claims 13-15 Morozumi discloses a transistor with a first conducting structure 43, for example, a signal/data line, upon a substrate 40; a second conducting

structure 44, for example a scanning/gate line, upon said substrate 40, with the projection of said second conducting structure (scanning/gate line 44) onto said substrate 40 intersecting the projection of said first conducting structure (signal/data line 43) onto said substrate 40; a third conducting structure 53, for example a source, upon said substrate 40 contacting with said first conducting structure (signal/data line 43), with the projection of said third conducting structure (source 53) onto said substrate 40 completely inside said projection of said second conducting structure (scanning/gate line 44) onto said substrate 40; a fourth conducting structure 50, for example a gate, upon said substrate 40, with the projection of said fourth conducting structure (gate 50) onto said substrate 40 separated from said projection of said first (signal/data line 43) and said third conducting structure (source 53) onto said substrate 40, said projection of said fourth conducting structure (gate 50) onto said substrate 40 completely inside said projection of said second conducting structure (scanning/gate line 44) onto said substrate 40; and said projection of said fourth conducting structure (gate 50) onto said substrate 40 approximately parallel to said projection of said third conducting structure (source 53) onto said substrate 40; a semiconductor layer, for example a channel region, upon said substrate 40 electrically coupling with said third (source 53) and said fourth conducting structure (gate 50), with the projection of said semiconductor layer (channel region 55) onto said substrate 40 completely inside said projection of said second conducting structure (scanning/gate line 44) onto said substrate 40; and a fifth conducting structure, for example a drain, drain electrode, or pixel electrode, upon said substrate

40 contacting with said fourth conducting structure (gate 50), with the projection of said fifth conducting structure (drain, drain electrode, or pixel electrode) onto said substrate 40 separated from said projection of said first (signal/data line 43) and said third conducting structure (source 53) onto said substrate 40, said projection of said fifth conducting structure (drain, drain electrode, or pixel electrode) onto said substrate 40 at least partly inside said projection of said second conducting structure (scanning/gate line 44) onto said substrate 40, said projection of said fifth (drain, drain electrode, or pixel electrode) and said third conducting structure (source 53) onto said substrate 40 on the opposite sides of said projection of said fourth conducting structure (gate 50) onto said substrate 40, and the side of said projection of said fourth conducting structure (gate 50) onto said substrate 40 facing said projection of said fifth conducting structure (drain, drain electrode, or pixel electrode) onto said substrate 40 only partly contacting with said projection of said fifth conducting structure (drain, drain electrode, or pixel electrode) onto said substrate 40, wherein the area of said projection of said fourth conducting structure (gate 50) onto said substrate 40 far larger than that of the overlap between said projection of said fifth (drain, drain electrode, or pixel electrode) and said second conducting structure (scanning/gate line 44). Note figures 4a, 4c, and column 4 lines 15-36 and 54-68 of Morozumi.

Allowable Subject Matter

6. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 1-5 and 7-9 have been considered but are moot in view of the new ground(s) of rejection.

8. With regard to claims 10,11 and 13-15, Applicant's arguments filed 01/27/2005 have been fully considered but they are not persuasive.

It is argued, at page 11 of the remarks, that "Morozumi '274 does not disclose 'said fourth conducting structure onto said substrate intersecting the projection of said third conducting structure onto said substrate' as in claims 1 and 10." However, claim 10 requires no such thing. It is noted that the features upon which applicant relies are not recited in the rejected claims 10,11, and 13-15. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is argued, at page 12 of the remarks, that "Morozumi '274 did not disclose that the 'fifth conducting structure upon said substrate, with the projection of said fifth conducting structure onto said substrate at 'least partly overlapping' said projection of said fourth

conducting structure onto said substrate and separated from said projection of said third, said first, and said second conducting structure onto said substrate' as in Claims 1 and 10." Claim 10 claims only four conducting structures. This argument makes no sense when applied to claim 10.

It is further argued, at page 12 of the remarks, that "Secondly, the claimed invention recited the 'projection of said fifth conducting structure onto said substrate partly overlapping said projection of said fourth conducting structure (gate electrode) onto said substrate and separated from said projection of said third (source), said first (data line), and said second conducting structure (gate line) onto said substrate.' Morozumi '274 disclosed the drain is connected to the electrode, but did not disclose the drain (as fifth conducting structure) has a projection overlapping said projection of said gate electrode (fourth conducting structure). Thus, Morozumi '274 cannot anticipate the claimed invention. "

Applicant's use of the term "claimed invention" is ambiguous. Insofar as "claimed invention" might mean, "claims 1-5 and 7-9," Applicant's argument has merit and requires the application of new art (Busta 4,859,623). Insofar as "claimed invention" might mean, "claims 10-15," Applicant's argument lacks merit because none of claims 10-15 require a fifth conducting structure having a projection onto a substrate that partly overlaps the projection onto said substrate of a fourth conducting structure.

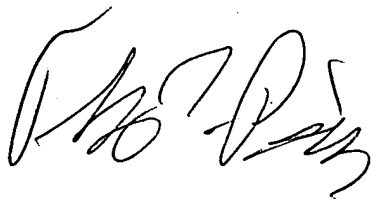
Conclusion

9. Because a new ground of rejection has been applied, this action is non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
03/05